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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,962	06/01/2001	James M. Reuter	P01-3663	4878

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EXAMINER	
NAWAZ, ASAD M	

ART UNIT	PAPER NUMBER
2155	

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,962	REUTER ET AL.	
	Examiner	Art Unit	
	Asad M. Nawaz	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Appeal Brief filed on July 18th, 2005. Claims 1-16 are pending.

Response to Arguments

2. Applicant's arguments, filed 7/18/05, with respect to claims 1-16 have been fully considered and are persuasive. The rejection of claims 1-16 has been withdrawn. The arguments, however, are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 recites the limitation "the host". There is insufficient antecedent basis for this limitation in the claim.

5. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim in general is not comprehendible.

6. Claims 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, it is not clear as to which entry the applicant is referring to in the limitation "...indicating states of the entry...".

7. Claims 12-16 recite the limitation "the storage segment" and "the write operation" in claim 12. There is insufficient antecedent basis for this limitation in the claim.

8. Claims 11-16 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Harish et al (USPN 5940850) hereinafter referred to as Harish.

As to claim 1, Harish teaches a virtual storage system for mapping virtual storage segments of differing sizes to storage locations, comprising:

an agent coupled to the host, the agent having volatile memory for storing a first table, (abstract; col 2, lines 25-34; RAM memory stores page table entries) the table having entries to map the virtual storage segments to the storage locations; (Abstract; col 2, lines 25-34; page table entries contain a mapping of virtual address to physical address)

and a controller coupled to the agent, the controller having non-volatile memory for storing a second table, (Abstract; col 2, lines 25-34; ROM memory stores page table entries) the controller intermittently causing contents of the first table to be replaced by

contents of the second table, (col 2, lines 10-19; the ROM data is loaded into RAM when memory is modified)

whereby during an input/output (I/O) operation, the host accesses one of the entries in the first table to determine one of the storage locations (Abstract; col 2, lines 12-34; the dynamic data as well as the page table entry is updated and a data page is also allocated).

Claim 7 is essentially the system for claim 1, however it contains the following additional limitations: a plurality of variables indicating states of the entry (Fig 3, col 4, lines 20-37) and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier (col 2, lines 19-51 and col 3, lines 56-67).

As to claim 2, Harish teaches the system of claim 1, wherein the second table identifies an alternate storage location within the storage locations (col 2, lines 10-51).

As to claim 3, Harish teaches the system of claim 2, wherein the second table further includes a bitmap that having entries that correspond to blocks of data stored within the alternate storage location (col 2, lines 10-51).

As to claim 4, Harish teaches the system of claim 1, further comprising an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments (col 2, lines 10-51).

As to claim 5, Harish teaches the system of claim 4, wherein an I/O operation accesses information on both the storage location and the alternative storage location (col 2, lines 10-51).

As to claim 6, Harish teaches the system of claim 5 wherein a bitmap designates blocks at the alternative storage location to use for the I/O operation (col 2, lines 10-51).

As to claim 8, Harish teaches the system of claim 7, wherein said first memory is a volatile memory (abstract; col 2, lines 10-51; RAM memory).

As to claim 9, Harish teaches the system of claim 7, wherein said second memory is a non-volatile memory (abstract; col 2, lines 10-51; ROM memory).

As to claim 10, Harish teaches the system of claim 7, wherein the states include a no-write state (abstract; col 2, lines 10-51).

As to claim 11, Harish teaches the system of claim 7, wherein the states include an error state (abstract; col 2, lines 10-51).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harish et al (USPN 5940850) further in view of Kuznetzov (USPN 5483649).

As to claim 12, Harish et al teaches a method for performing an input/output operation on a virtual storage segment defined by a first table that maps the storage segment to a first storage location, the method comprising: identifying portions of the

virtual storage segment to be effected during the write operation; (col 2, lines 19-51 and col 3, lines 56-67).

storing a record of the identified portions at a second table and not at the first table (col 2, lines 19-51).

and writing to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions (col 2, lines 19-51 and col 3, lines 56-67).

However, Harish does not explicitly indicate turning off input/output operations at the first storage location.

Kuznetzov teaches turning off input/output operations at the first storage location (col 2, lines 14-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Kuznetzov into those of Harish in order to make the system more secure. Allowing various input/output operations to be enabled at the first storage location would make the system susceptible to numerous deficiencies, including system and/or data corruption.

As to claim 13, Kuznetzov teaches the method of claim 12, wherein the turning off step includes activating an invalid state (col 2, lines 14-30).

As to claim 14, Harish teaches the method of claim 12, wherein a subsequent read operation for the virtual segment occur at portions of the first storage location not included in the identified portions and the portions of the second storage location associated with the identified portions (col 2, lines 19-51 and col 3, lines 56-67).

As to claims 15, Harish teaches the method of claim 14, wherein the first table is stored by an agent and during the read operation, the record of the identified portions is sent to the agent (col 2, lines 19-51 and col 3, lines 56-67).

As to claim 16, Harish teaches the method of claim 15, wherein the mapping between the virtual storage segment and first storage location is contained in numerous first tables, each of the first table stored by a different agent (col 2, lines 19-51 and col 3, lines 56-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asad M. Nawaz whose telephone number is (571) 272-3988. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on (571) 272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMN

SALEH NAJJAR
PRIMARY EXAMINER